C8051F390-GDI

Tested 50 MIPS 16 kB Flash Mixed-Signal MCU Die in Wafer Form

Analog Peripherals
- **10-Bit ADC**
  - Programmable throughput up to 500 ksps
  - Up to 16 external inputs, programmable as single-ended or differential
  - Reference from on-chip voltage reference, V_{DD} or external VREF pin
  - Internal or external start of conversion sources
- **Two 10-Bit Current Output DACs**
  - Supports output through resets for continuous operation
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
- **Precision Temperature Sensor**
  - Accurate to ±2 °C across temperature range with no user calibration

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers

Low Power
- 160 µA/MHz Active mode with 49 MHz internal precision oscillator
- 200 nA Stop mode current

Temperature Range
- –40 to +105 °C

Supply Voltage 1.8 to 3.6 V
- Built-in voltage supply monitor

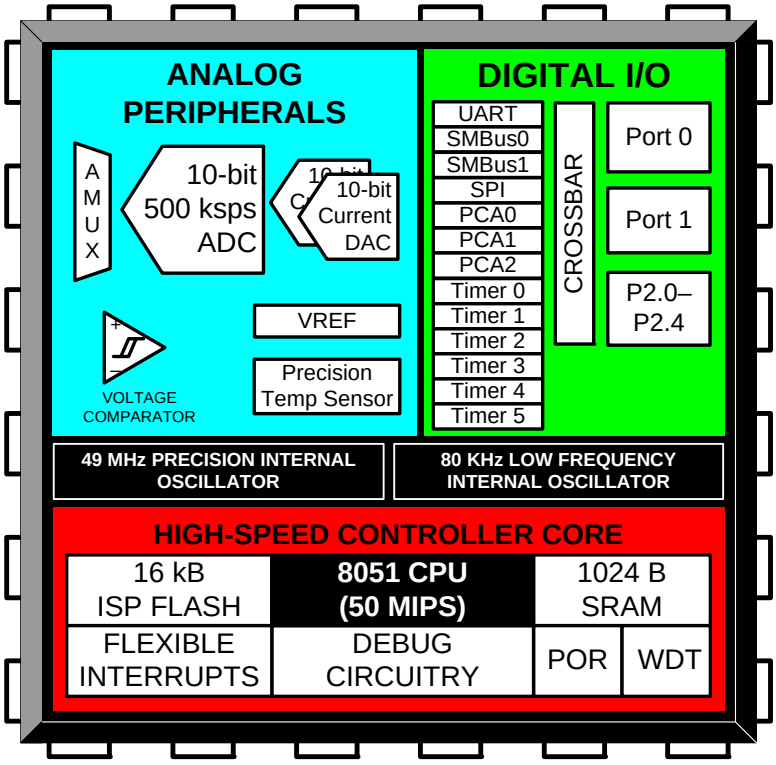
High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

Memory
- 1 kB internal data RAM (256 + 768)
- 16 kB Flash; In-system programmable in 512-byte Sectors

Digital Peripherals
- 21 Port I/O
- UART, 2 SMBus (I^2C compatible), and SPI serial ports
- Six general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules and PWM functionality

Clock Sources
- 49 MHz ±2% precision internal oscillator
  - Supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
- 80 kHz low-frequency, low-power oscillator
- External oscillator: Crystal, RC, C, or CMOS clock
- Can switch between clock sources on-the-fly; useful in power saving modes

Full Technical Data Sheet
- C8051F39x-37x



1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kBytes)	RAM (kBytes)	49 MHz Internal Oscillator	80 kHz Internal Oscillator	SMBus/I^2C	UART	SPI	Timers (16-bit)	PWM / PCA Channels	Digital Port I/Os	ADC Input Channels	Precision Temperature Sensor	Voltage Reference	IDAC Output Channels	Analog Comparators	Wafer Thickness
C8051F390-A-G1DI	50	16	1	1	1	2	1	1	6	3	21	20	2	2	2	1	28.5433 mil / 725 µm (No backgrind)
C8051F390-A-GDI	50	16	1	1	1	2	1	1	6	3	21	20	2	2	2	1	12 mil (backgrind)

2. Pin Definitions

Table 2.1 lists the pin definitions for the C8051F390-GDI. For a full description of each pin, refer to the C8051F39x-C8051F37x data sheet.

Table 2.1. Pin Definitions for the C8051F390-GDI

Name	Physical Pad Number	Type	Description
V_{DD}	5		Power Supply Voltage.
V_{DD}	6		Power Supply Voltage.
GND	3		Ground. This ground connection is required. The center pad may optionally be connected to ground also.
GND	4		Ground. This ground connection is required. The center pad may optionally be connected to ground also.
$\overline{\text{RST}}$/ C2CK	7	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 10 µs. Clock signal for the C2 Debug Interface.
P2.4 / C2D	8	D I/O D I/O	P2.4. Bi-directional data signal for the C2 Debug Interface.
P0.0/ VREF	2	D I/O or A In A In	Port 0.0. External VREF input.
P0.1 IDA0	1	D I/O or A In A Out	Port 0.1. IDA0 Output.
P0.2/ XTAL1	33	D I/O or A In A In	Port 0.2. External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/ XTAL2	32	D I/O or A In A I/O or D In	Port 0.3. External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.

Table 2.1. Pin Definitions for the C8051F390-GDI

Name	Physical Pad Number	Type	Description
P0.4	31	D I/O or A In	Port 0.4.
P0.5	30	D I/O or A In	Port 0.5.
P0.6/ CNVSTR	29	D I/O or A In D In	Port 0.6. ADC0 External Convert Start or IDA0 Update Source Input.
P0.7	28	D I/O or A In	Port 0.7.
P1.0	26	D I/O or A In	Port 1.0.
P1.1	25	D I/O or A In	Port 1.1.
P1.2 IDA1	24	D I/O or A In A Out	Port 1.2. IDA1 Output.
P1.3	23	D I/O or A In	Port 1.3.
P1.4	22	D I/O or A In	Port 1.4.
P1.5	20	D I/O or A In	Port 1.5.
P1.6	19	D I/O or A In	Port 1.6.
P1.7	18	D I/O or A In	Port 1.7.
P2.0	17	D I/O or A In	Port 2.0.
P2.1	14	D I/O or A In	Port 2.1.
P2.2	13	D I/O or A In	Port 2.2.
P2.3	9	D I/O or A In	Port 2.3.

3. Bonding Instructions

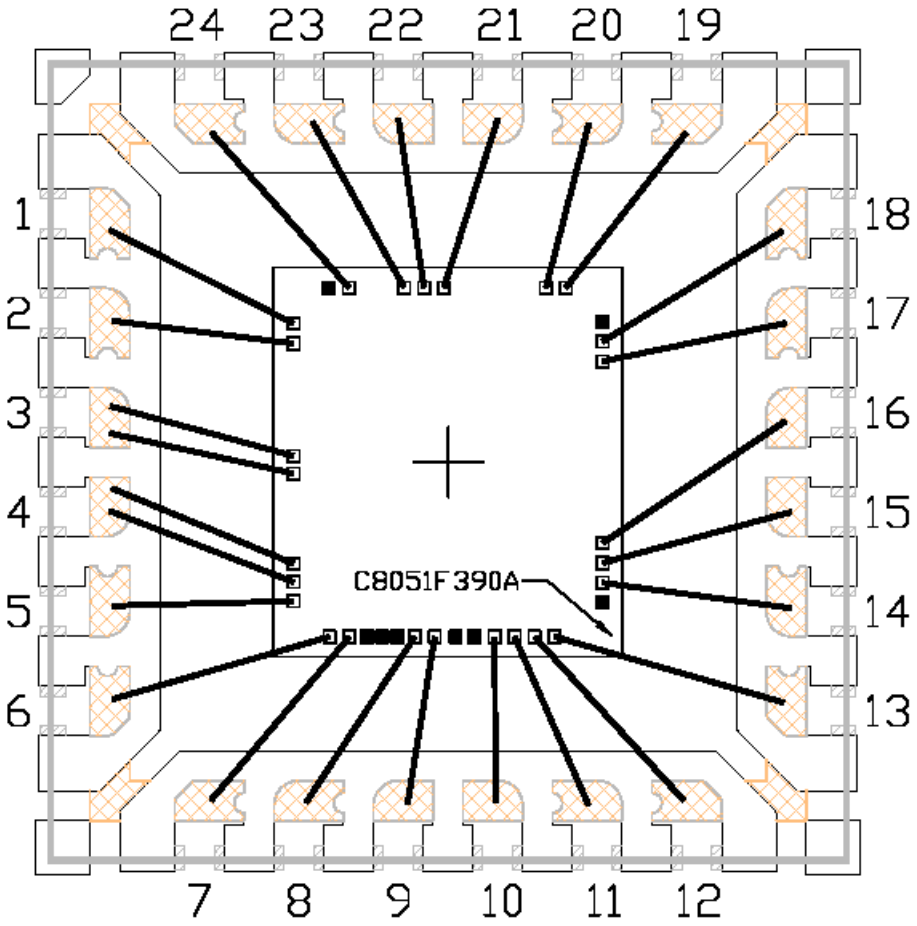


Figure 3.1. Die Bonding Example (QFN-24)

Table 3.1. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (QFN-24)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
1	1	P0.1/IDA0	–696	–777
2	2	P0.0/VREF	–596	–777
3	3	GND	–31	–777
4	3	GND	57	–777
5	4	V_{DD}	510	–777
6	4	V_{DD}	602	–777
***Note:** Pins marked “Reserved” should not be connected.				

Table 3.1. Bond Pad Coordinates (Relative to Center of Die) (Continued)

Physical Pad Number	Example Package Pin Number (QFN-24)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
7	5	$\overline{\text{RST}}$/C2CK	698	–777
8	6	P2.4/C2D	877	–596
9	7	P2.3	877	–496
10	Reserved		877	–407
11	Reserved		877	–332
12	Reserved		877	–257
13	8	P2.2	877	–167
14	9	P2.1	877	–67
15	Reserved		877	38
16	Reserved		877	129
17	10	P2.0	877	235
18	11	P1.7	877	335
19	12	P1.6	877	435
20	13	P1.5	877	535
21	Reserved		702	777
22	14	P1.4	606	777
23	15	P1.3	506	777
24	16	P1.2/IDA1	406	777
25	17	P1.1	–506	777
26	18	P1.0	–606	777
27	Reserved		–702	777
28	19	P0.7	–877	592
29	20	P0.6/CNVSTR	–877	492
30	21	P0.5	–877	–21
31	22	P0.4	–877	–121
32	23	P0.3/XTAL2	–877	–221
33	24	P0.2/XTAL1	–877	–499
34	Reserved		–877	–599

***Note:** Pins marked “Reserved” should not be connected.

Table 3.2. Wafer and Die Information

Wafer ID	C8051F390A
Wafer Dimensions	8 in
Die Dimensions	1.72 mm x 1.92 mm
Wafer Thickness (No backgrind)	28.5433 mil ±1 mil (725 µm)
Wafer Thickness (With backgrind)	12 mil ±1 mil
Wafer Identification	Notch
Scribe Line Width	60 µm
Die Per Wafer*	Contact Sales For Info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 µm
***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

4. Wafer Storage Guidelines

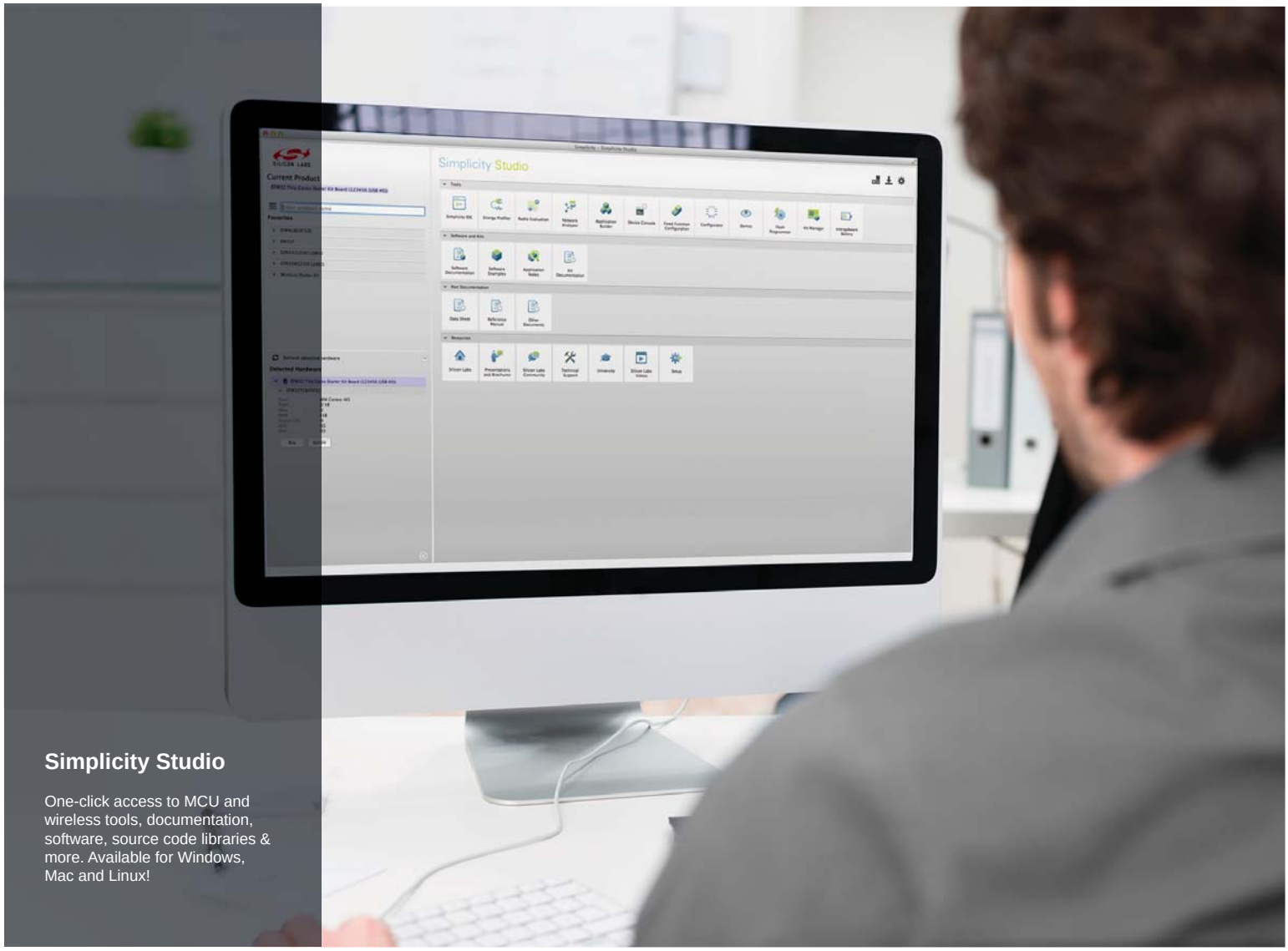
It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

5. Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet this requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, backgrind or are on tape. Initial response time for FA requests that meet this requirements will be 3 weeks.



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